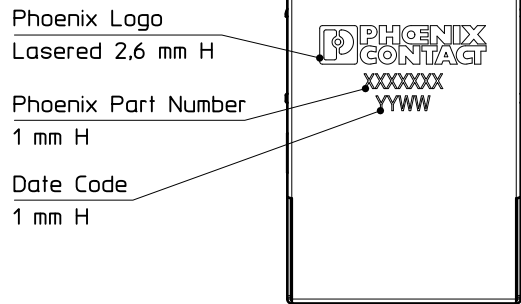
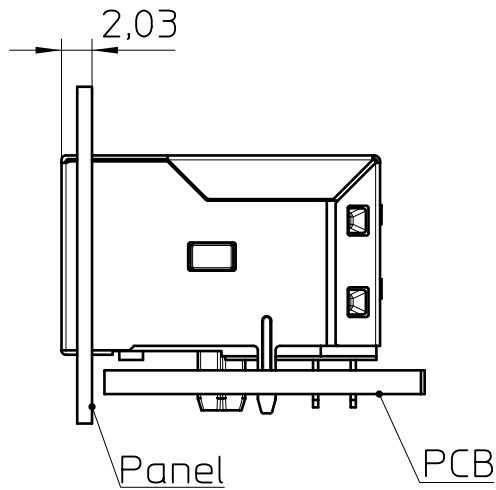
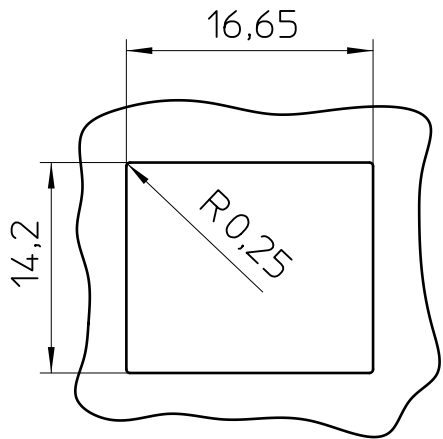


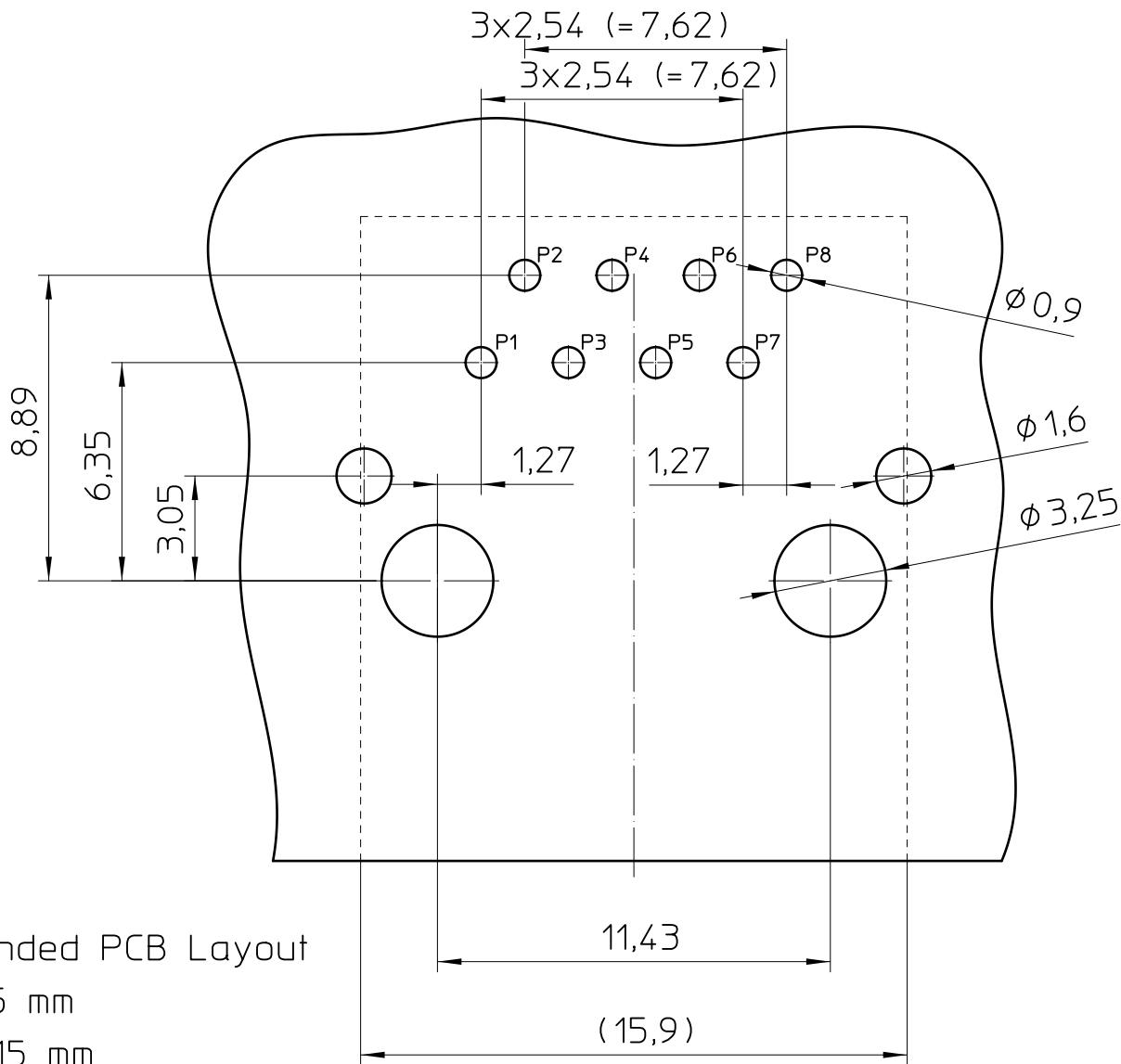
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Recommended panel cutout



PCB drill hole dimensions (see from component side)



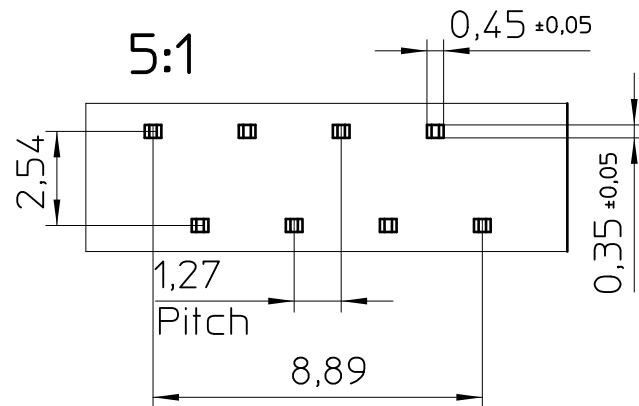
Recommended PCB Layout

Tol: ±0,05 mm

T=1,60±0,15 mm

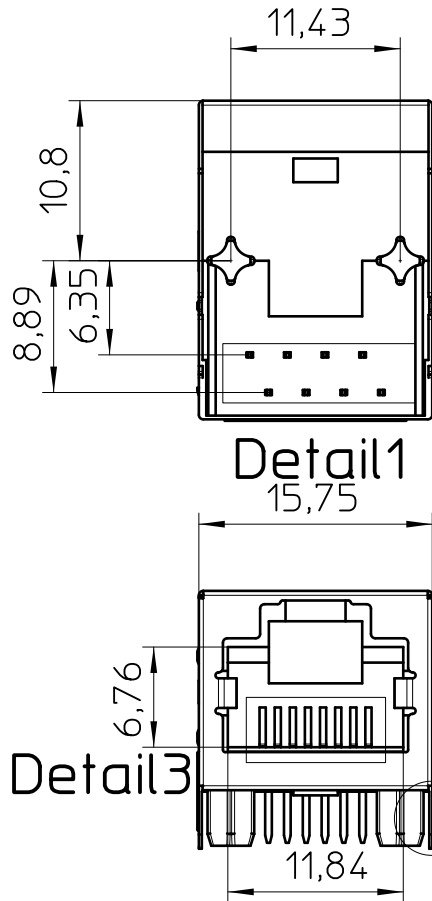
Detail1

5:1



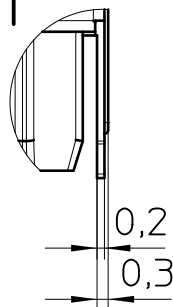
Detail1

15,75

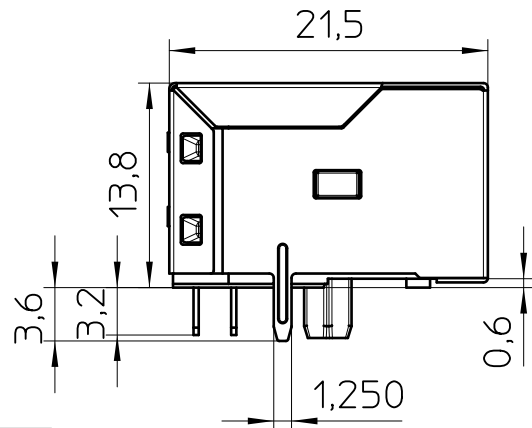


Detail2

5:1

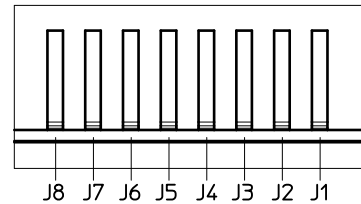


Detail2



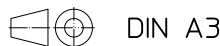
Detail3

5:1



General Tolerances

1 Decimal Place	±0,25
2 Decimal Places	±0,20
3 Decimal Places	±0,15



page 1 of 2

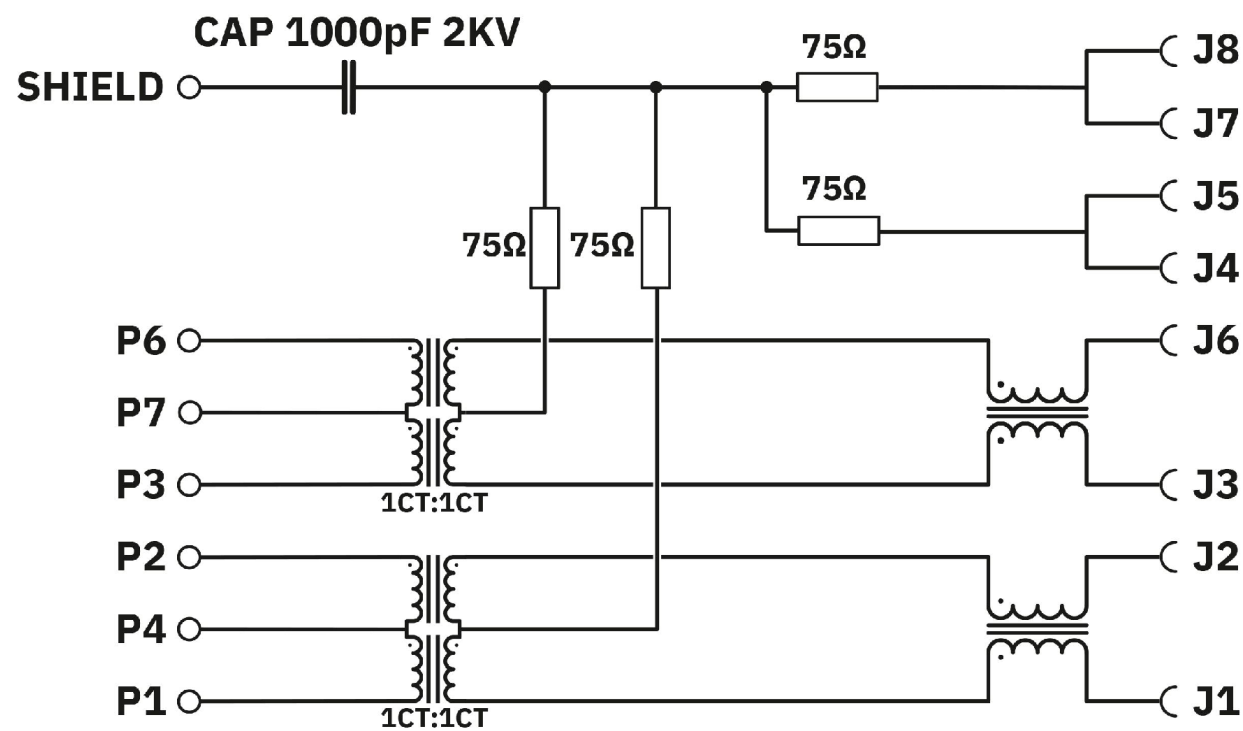
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date	document-type		
07.11.2024	TECDOC 2D_Productfamily		
description			CUC-IB5M-J1ST-AT/R4T

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PCB SIDE

JACK SIDE



ELECTRONICAL SPECIFICATIONS

1. ACCORDING TO IEEE 802.3

2. TURN RATIO @100KHz: (P1~P2):(J1~J2) = 1:1±5%
(P3~P6):(J3~J6) = 1:1±5%

3. PRIMARY INDUCTANCE: 350μH MIN @100KHz
0,1V 8mA DC BIAS

4. DC RESISTANCE: 1,2 OHMS MAX

5. INSERTION LOSS: 1-100MHz -1,2dB MAX

6. RETURN LOSS: 1-30MHz -16dB MIN
30-60MHz -12dB MIN
60-80MHz -10dB MIN

7. CROSS TALK: 1-100MHz -30dB MIN

8. COMMON TO COMMON
MODE ATTENUATION: 1-100MHz -30dB MIN

9. ISOLATION: PHY SIDE TO LINE SIDE: 1500VAC or 2250VDC

- EN ISO 291 23/50

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		date 07.11.2024		document-type TECDOC 2D_Productfamily					
page 2		of 2		description CUC-IB5M-J1ST-AT/R4T					