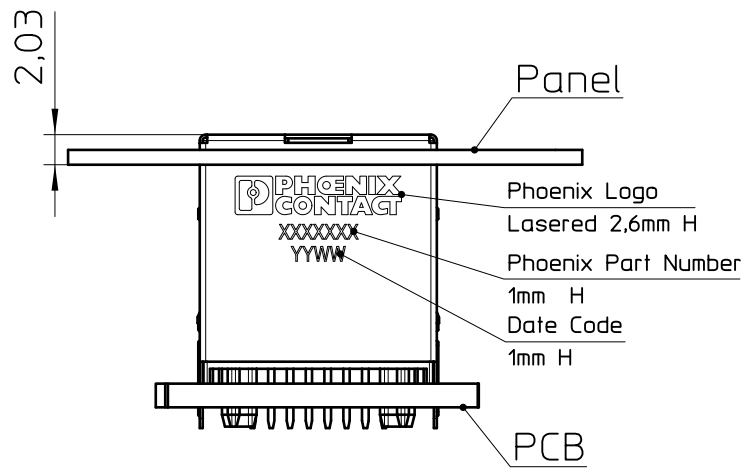
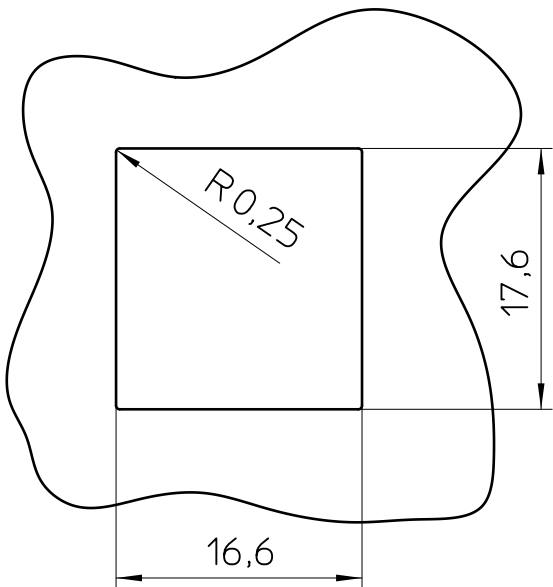


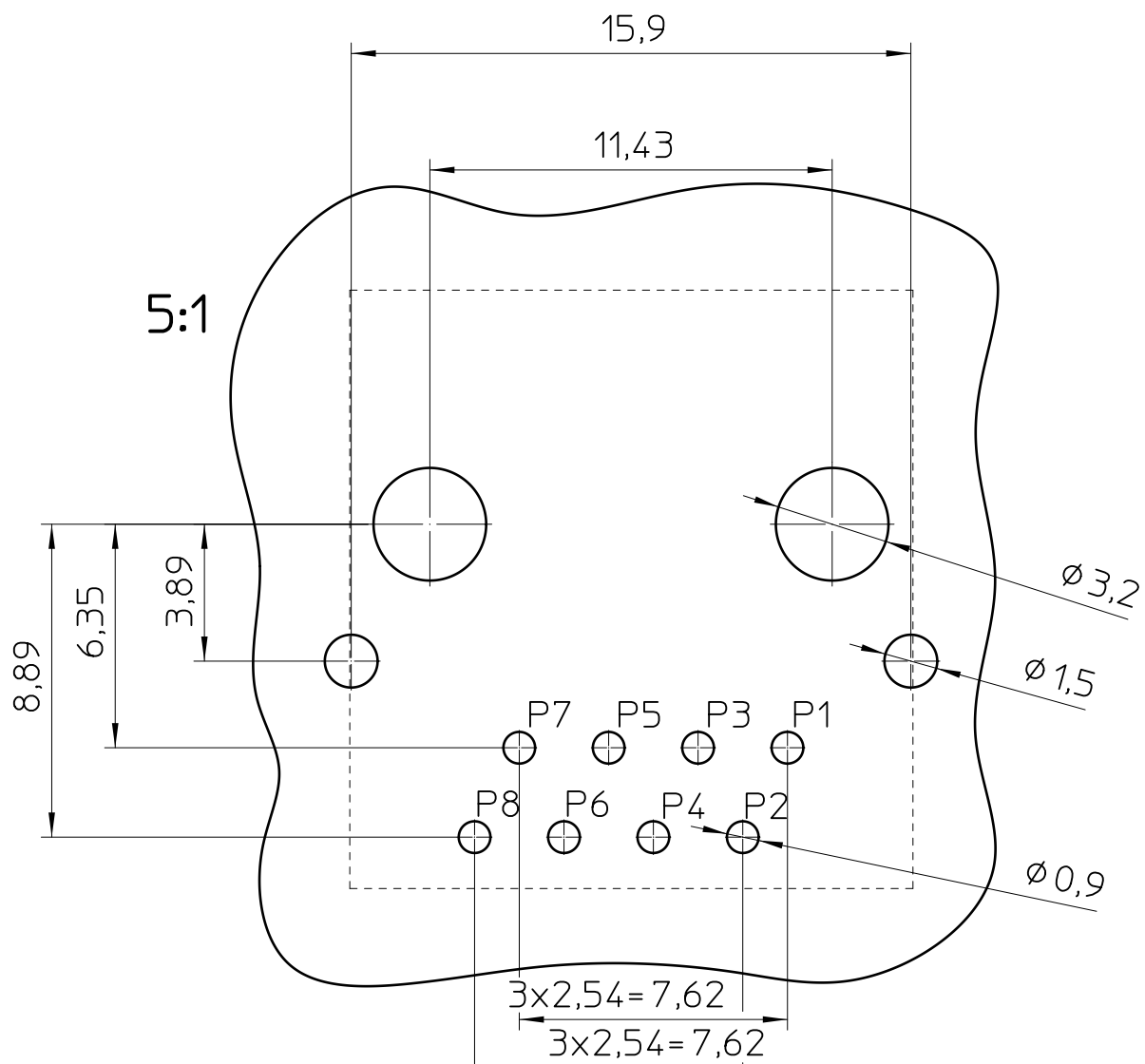
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Recomended panel cutout

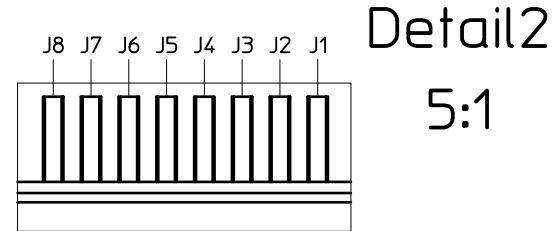
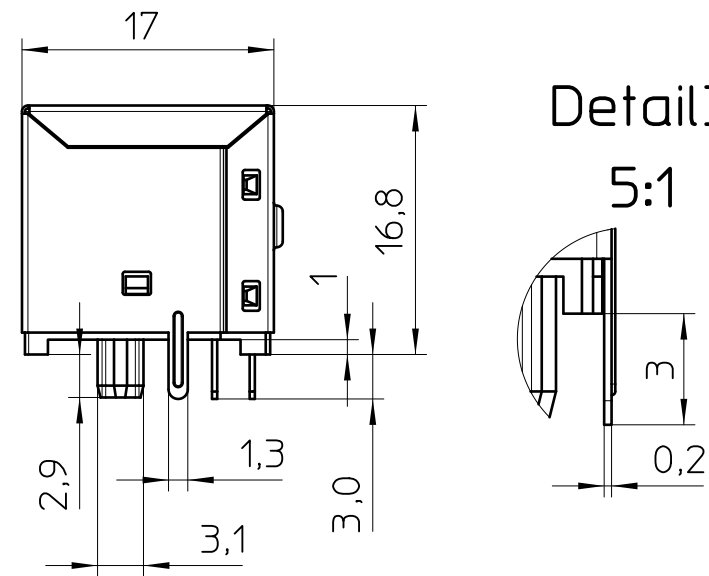
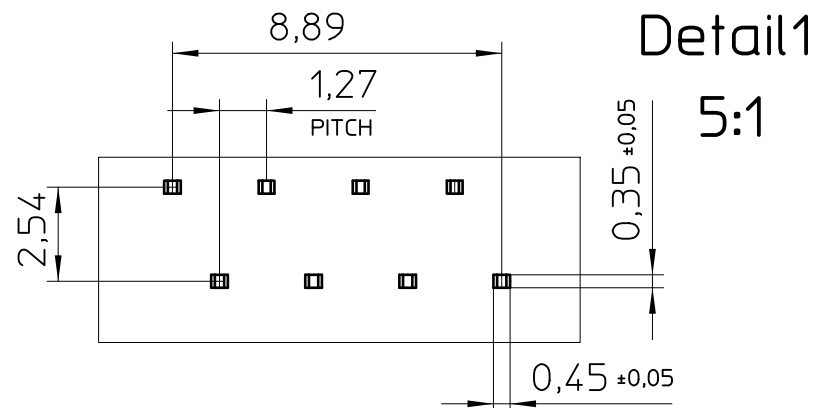
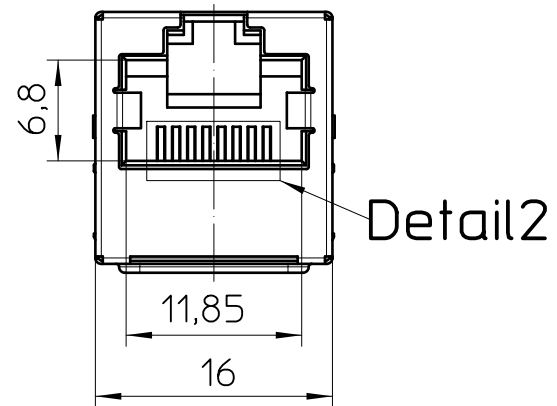
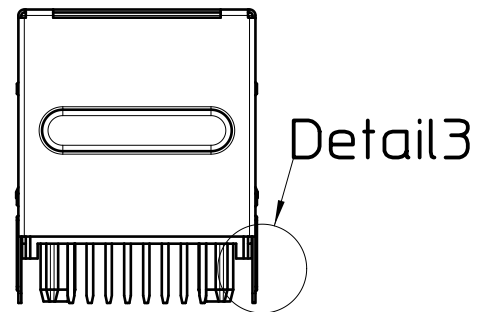
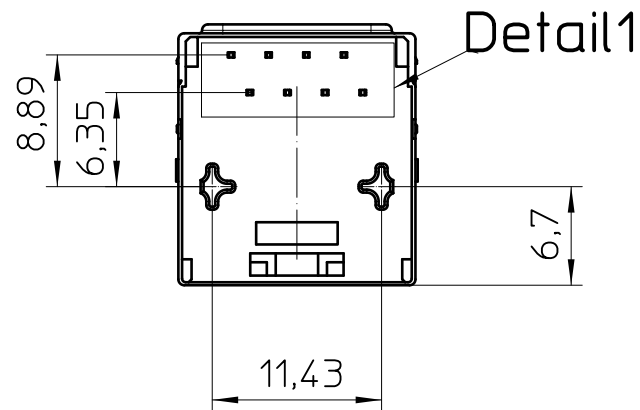


PCB drill hole dimensions (see from component side)



Recommended PCB Layout (Tol: ±0,05, T=1,60±0,15mm)

PCB thickness: 1,6mm



General Tolerances

1 Decimal Place	±0,25
2 Decimal Places	±0,20
3 Decimal Places	±0,15



page 1 of 2

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TECDOC 2D_Productfamily

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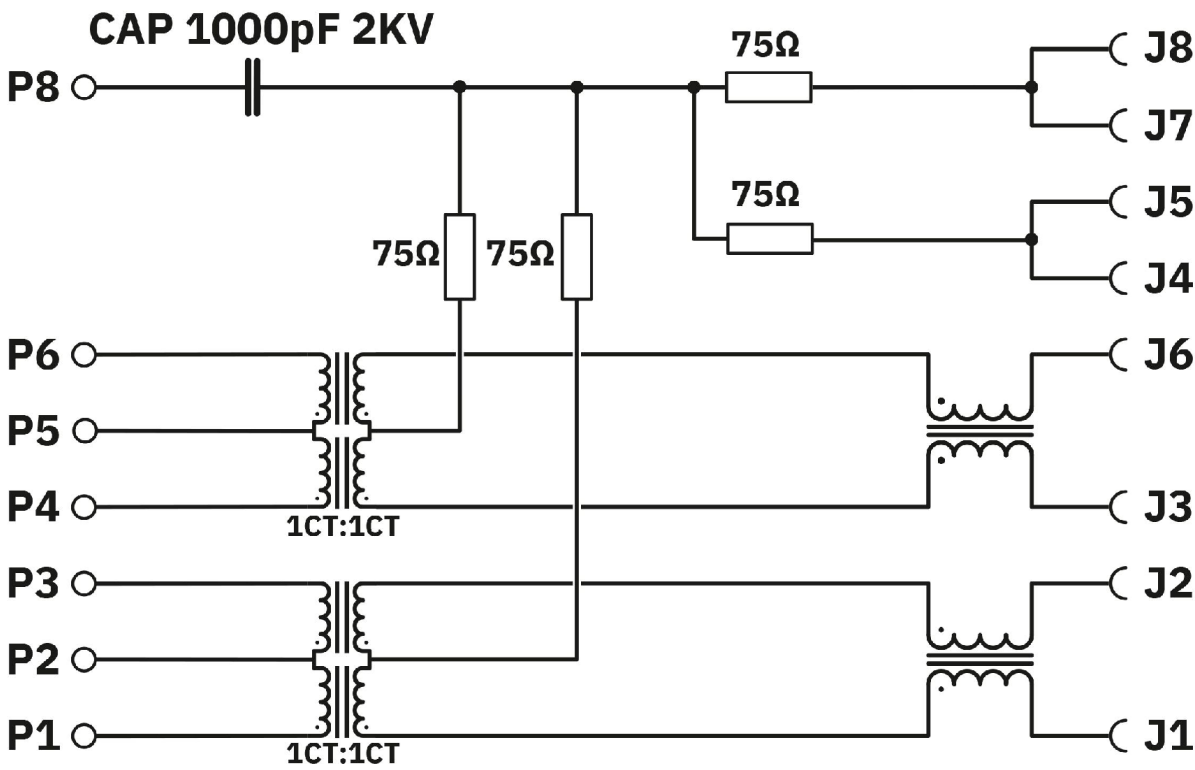
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PCB SIDE



JACK SIDE

ELECTRONICAL SPECIFICATIONS

- 1. ACCORDING TO IEEE 802.3**
- 2. TURN RATIO @100KHz:** (P1~P3):(J1~J2) = 1:1±5%
(P4~P6):(J3~J6) = 1:1±5%
- 3. PRIMARY INDUCTANCE:** 350μH MIN @100KHz
0,1V 8mA DC BIAS
- 4. DC RESISTANCE:** 1,2 OHMS MAX
- 5. INSERTION LOSS:** 1-100MHz -1,2dB MAX
- 6. RETURN LOSS:** 1-30MHz -16dB MIN
30-60MHz -12dB MIN
60-80MHz -10dB MIN
- 7. CROSS TALK:** 1-100MHz -30dB MIN
- 8. COMMON TO COMMON MODE ATTENUATION:** 1-100MHz -30dB MIN
- 9. ISOLATION: PHY SIDE TO LINE SIDE: 1500VAC or 2250VDC**

- EN ISO 291 23/50

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