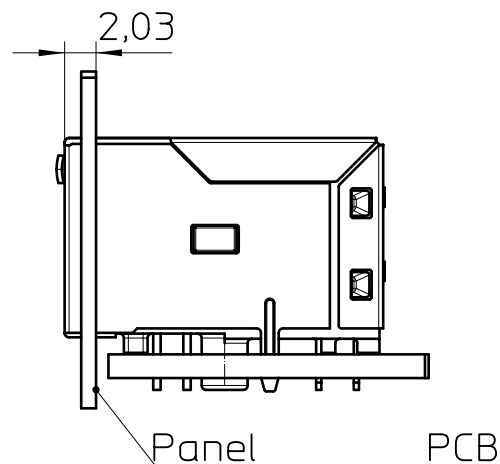
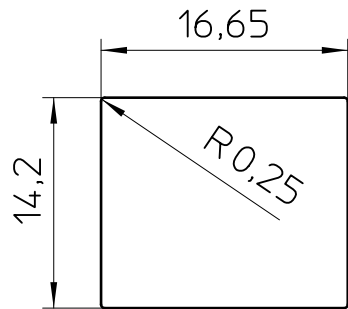


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Recommended panel cutout



Phoenix Logo

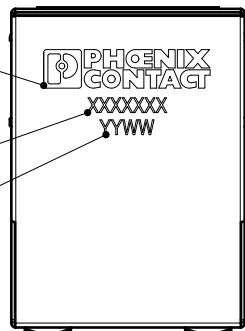
Lasered 2,6 mm H

Phoenix Part Number

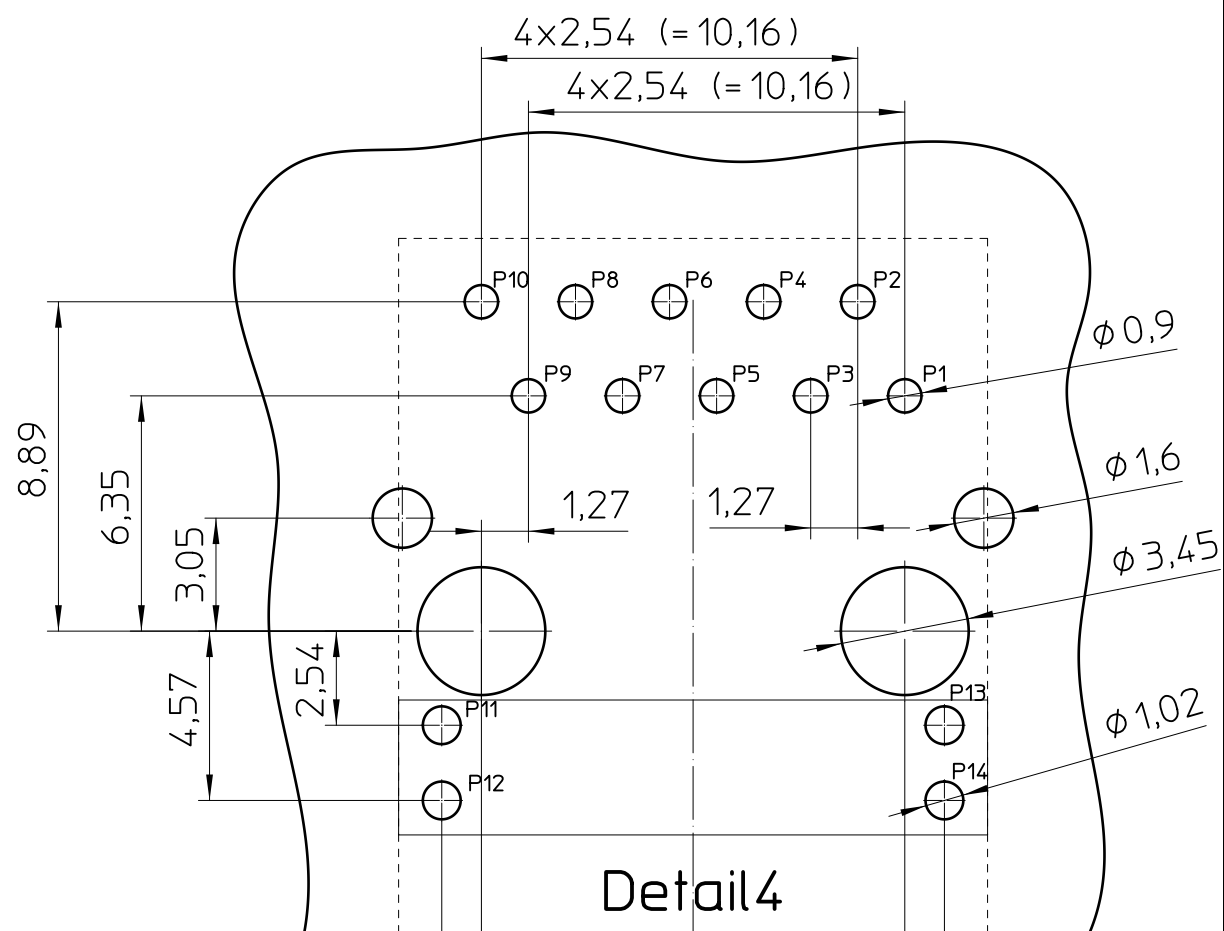
1 mm H

Date Code

1 mm H



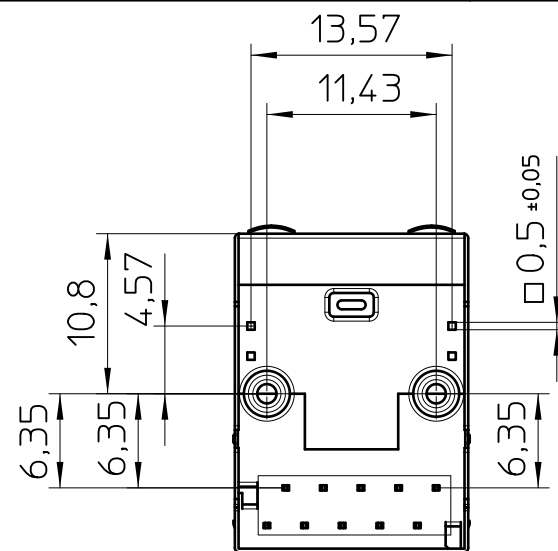
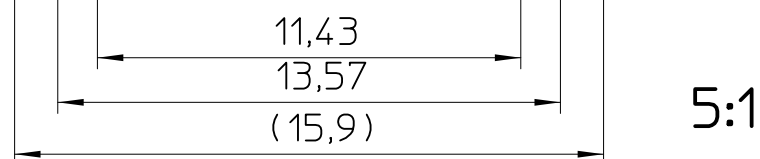
PCB drill hole dimensions (see from component side)



Recommended PCB Layout

Tol: ±0,05 mm

T=1,60±0,15 mm



Detail1

15,75

Detail3

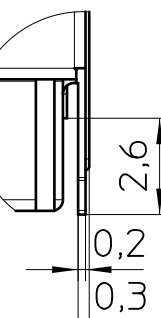
8,5

LED 1
GREEN

LED 2
YELLOW

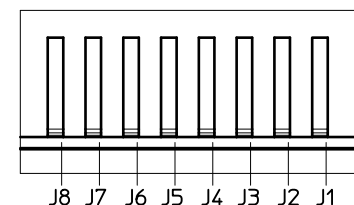
Detail2

11,84



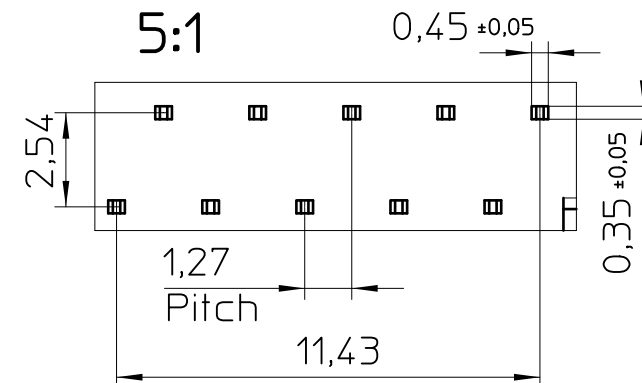
Detail3

5:1



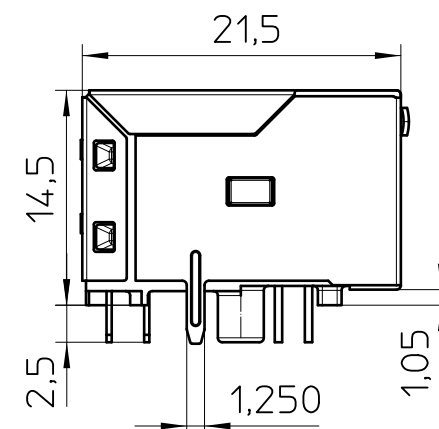
Detail1

5:1



Detail2

5:1



Detail4

5:1

LED 1
GREEN
⊕ P11
⊖ P12

LED 2
YELLOW
⊕ P13
⊖ P14

LED-Specifications

LED	Forward Voltage (max)	*Forward Voltage (Typical)
GREEN	2,4 V	2,2 V
YELLOW	2,5 V	2,1 V

*Forward DC current: 20 mA

General Tolerances

1 Decimal Place	±0,25
2 Decimal Places	±0,20
3 Decimal Places	±0,15

DIN A3



page 1 of 2

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01760856 / 00 1663982

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07.11.2024

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TECDOC 2D_Productfamily

description
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scale
2:1

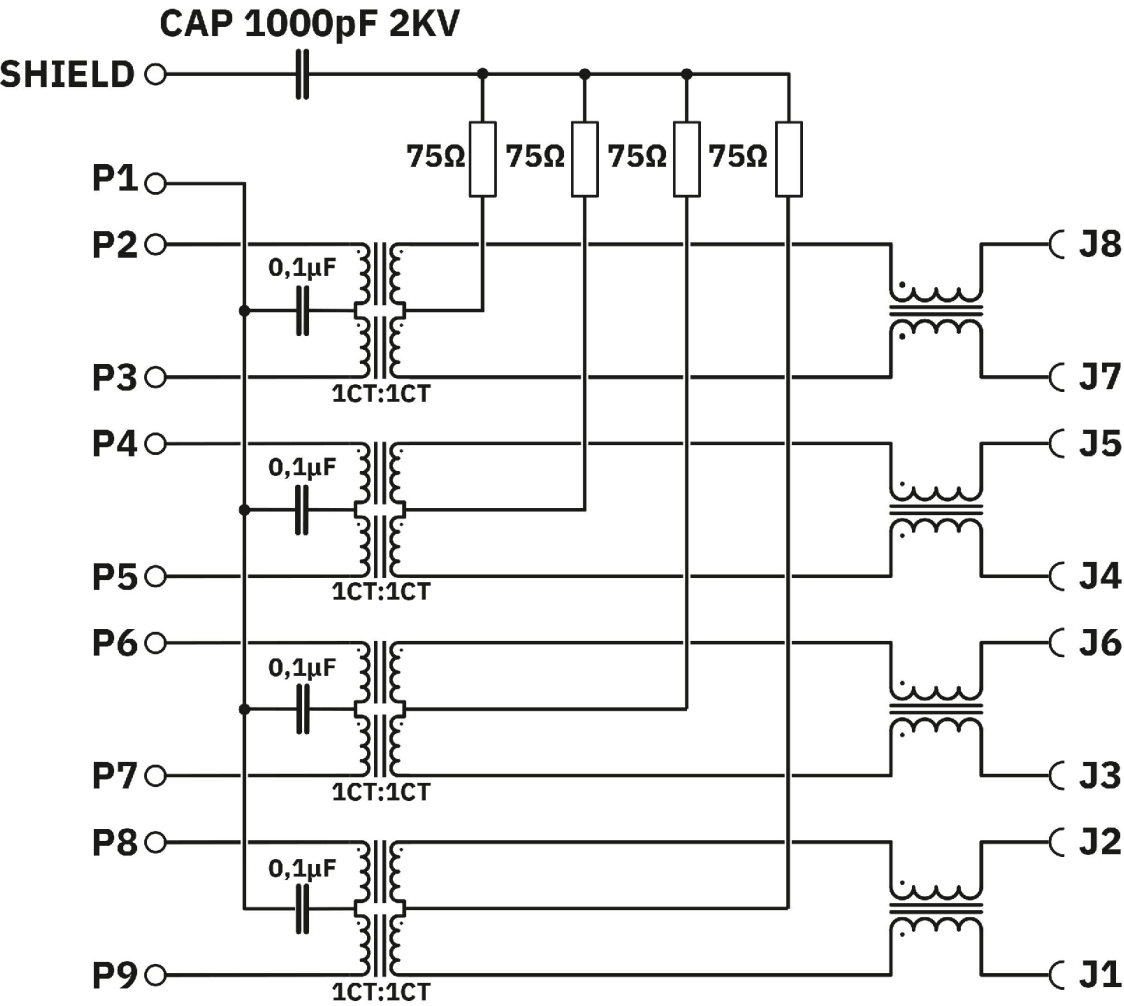
- Simplified representation
- Document excluded
from change process
- Linear dimensions [mm]

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PCB SIDE

JACK SIDE



ELECTRONICAL SPECIFICATIONS

1. ACCORDING TO IEEE 802.3
2. TURN RATIO @100KHz: (P2~P3):(J1~J2) = 1:1±5%
(P4~P5):(J3~J6) = 1:1±5%
(P6~P7):(J4~J5) = 1:1±5%
(P8~P9):(J7~J8) = 1:1±5%
3. PRIMARY INDUCTANCE: 350μH MIN @100KHz
0,1V 8mA DC BIAS
4. DC RESISTANCE: 1,2 OHMS MAX
5. INSERTION LOSS: 1-100MHz -1,0dB MAX
100-125MHz -1,2dB MAX
6. RETURN LOSS: 1-40MHz -16dB MIN
40-60MHz -12dB MIN
60-80MHz -10dB MIN
80-100MHz -8dB MIN
7. CROSS TALK: 1-100MHz -30dB MIN
8. COMMON TO COMMON MODE ATTENUATION: 1-100MHz -30dB MIN
9. ISOLATION: PHY SIDE TO LINE SIDE: 2250VDC

- EN ISO 291 23/50

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	07.11.2024	TECDCOC 2D_Productfamily		
	description			
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