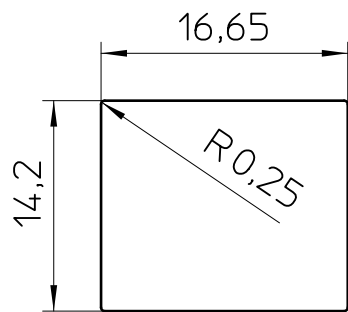


Transfer or duplication of this document as well as the utilisation or communication of its content are not permitted unless express consent is granted. Violations give rise to claims for damages. All rights reserved in case of patent, utility model or design patent registrations. Tolerance specifications do not include clearances inherent in the design.

Weitergabe sowie Vervielfältigung dieses Dokuments, Verwertung und Mitteilung seines Inhalts sind verboten, soweit nicht ausdrücklich gestattet. Zuwiderhandlungen verpflichten zu Schadensersatz. Alle Rechte für den Fall der Patent-, Gebrauchsmuster- oder Designeintragung vorbehalten. Baugründingtes Spiel ist in den Toleranzangaben nicht berücksichtigt.

Recommended panel cutout



Phoenix Logo

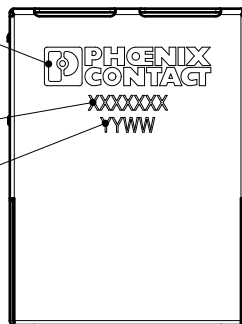
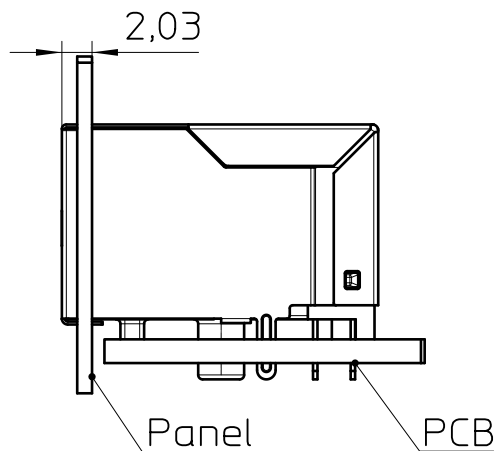
Lasered 2,6 mm H

Phoenix Part Number

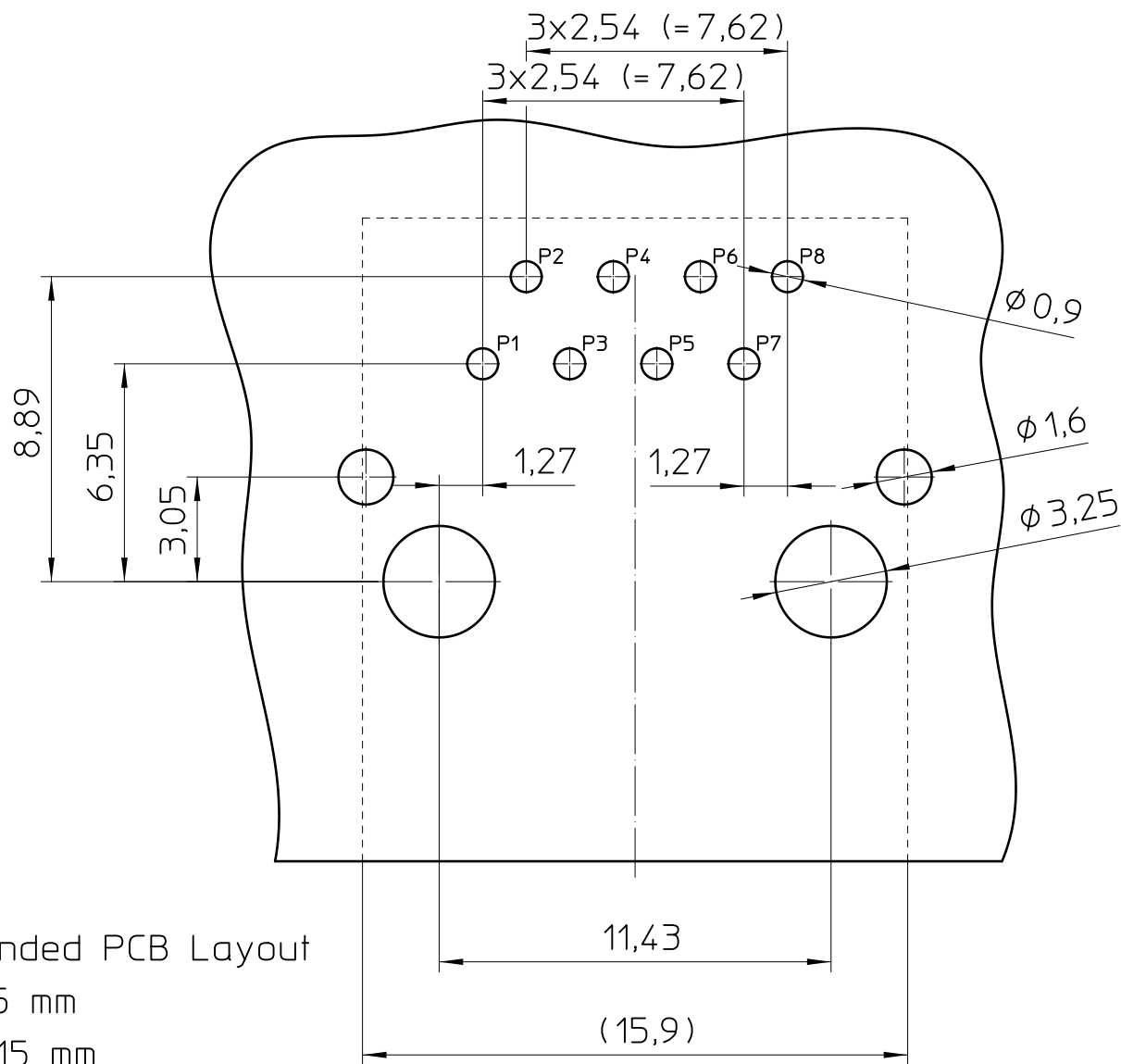
1 mm H

Date Code

1 mm H



PCB drill hole dimensions (see from component side)



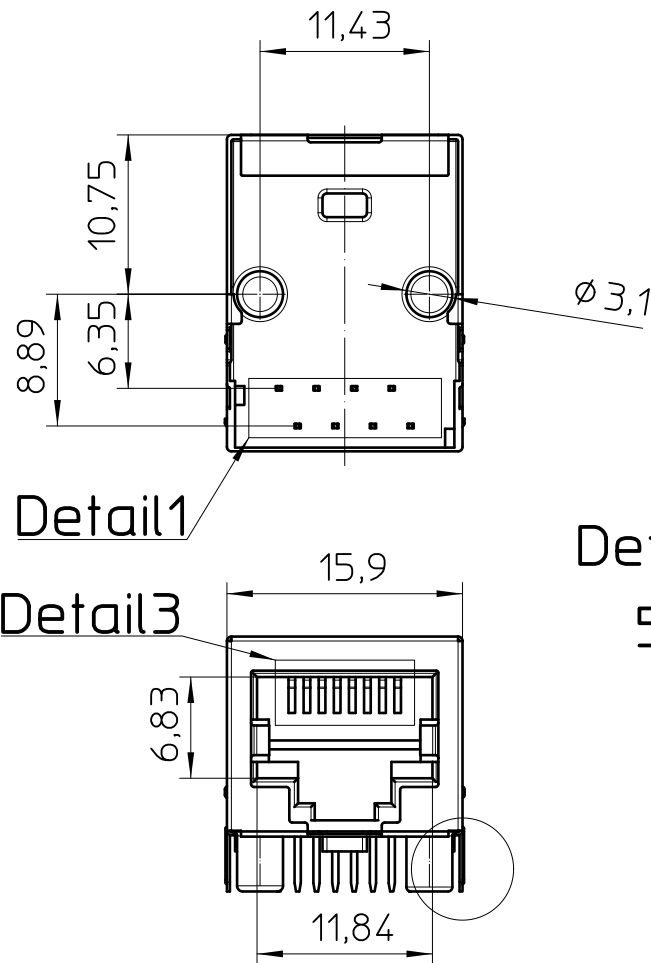
Recommended PCB Layout

Tol: ±0,05 mm

T=1,60±0,15 mm

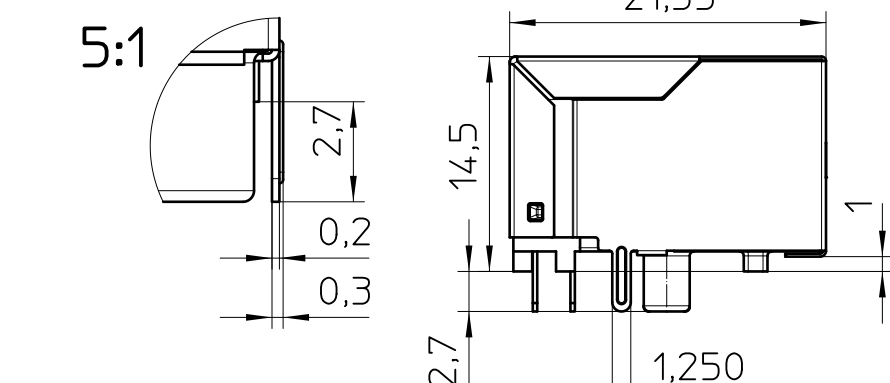
Detail1

Detail3



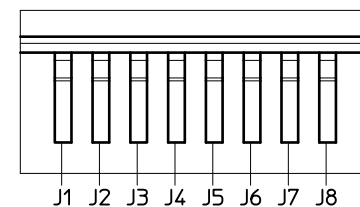
Detail2

5:1



Detail3

5:1



General Tolerances

1 Decimal Place	±0,25
2 Decimal Places	±0,20
3 Decimal Places	±0,15



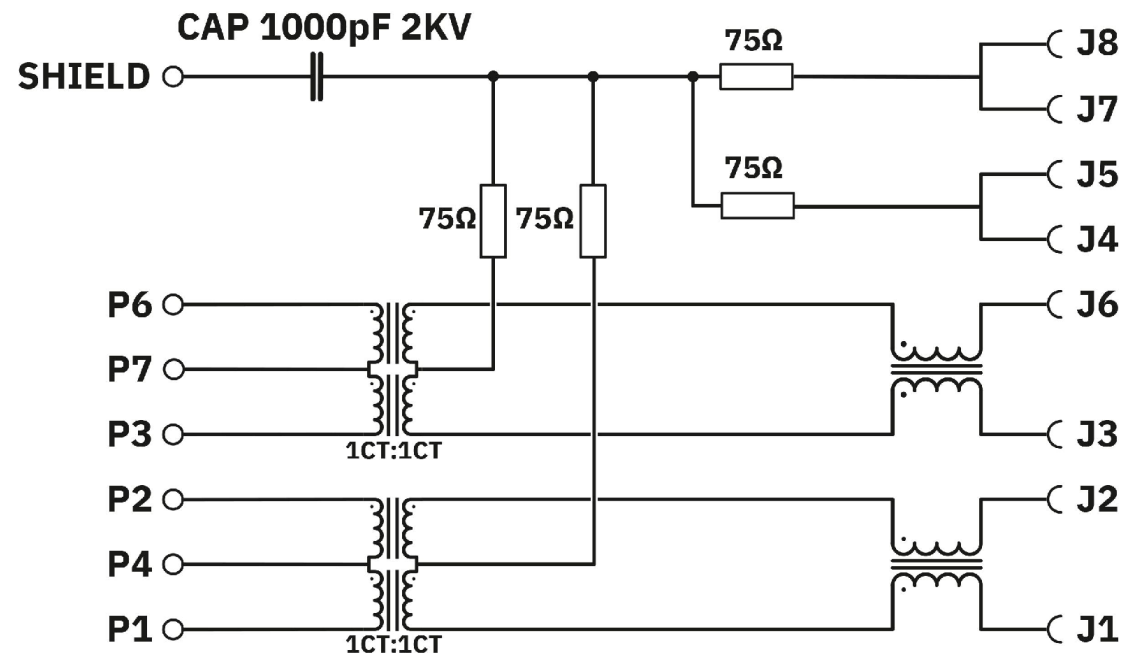
page 1 of 2

document-no. / ri		article-no.	scale	- Simplified representation - Document excluded from change process - Linear dimensions [mm]
01739055 / 00		1664055	2:1	
date	document-type			
04.11.2024	TECDOC 2D_Productfamily			
description				
CUC-IA4M-J1ST-AB/R4R				

Transfer or duplication of this document as well as the utilisation or communication of its content are not permitted unless express consent is granted. Violations give rise to claims for damages. All rights reserved in case of patent, utility model or design patent registrations. Tolerance specifications do not include clearances inherent in the design.

Weitergabe sowie Vervielfältigung dieses Dokuments, Verwertung und Mitteilung seines Inhalts sind verboten, soweit nicht ausdrücklich gestattet. Zuwiderhandlungen verpflichten zu Schadenersatz. Alle Rechte für den Fall der Patent-, Gebrauchsmuster- oder Designeintragung vorbehalten. Bauartbedingtes Spiel ist in den Toleranzangaben nicht berücksichtigt.

PCB SIDE



JACK SIDE

ELECTRONICAL SPECIFICATIONS

- 1. ACCORDING TO IEEE 802.3**
- 2. TURN RATIO @100KHz:** (P1~P2):(J1~J2) = 1:1±5%
(P3~P6):(J3~J6) = 1:1±5%
- 3. PRIMARY INDUCTANCE:** 350μH MIN @100KHz
0,1V 8mA DC BIAS
- 4. DC RESISTANCE:** 1,2 OHMS MAX
- 5. INSERTION LOSS:** 1-100MHz -1,2dB MAX
- 6. RETURN LOSS:** 1-30MHz -16dB MIN
30-60MHz -12dB MIN
60-80MHz -10dB MIN
- 7. CROSS TALK:** 1-100MHz -30dB MIN
- 8. COMMON TO COMMON MODE ATTENUATION:** 1-100MHz -30dB MIN
- 9. ISOLATION: PHY SIDE TO LINE SIDE: 1500VAC or 2250VDC**

- EN ISO 291 23/50

 DIN A3	document-no. / ri	article-no.	scale	- Simplified representation - Document excluded from change process - Linear dimensions [mm]
	01739055 / 00	1664055	2:1	
	date	document-type		
	04.11.2024	TECDOC 2D_Productfamily		
	description			
page 2	of 2	CUC-IA4M-J1ST-AB/R4R		