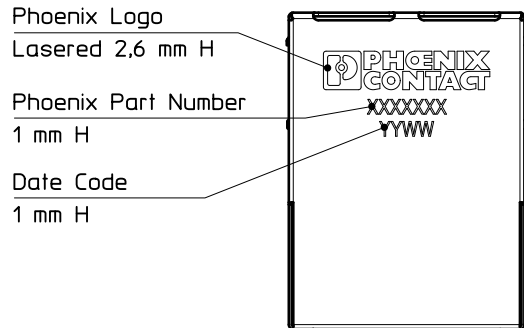
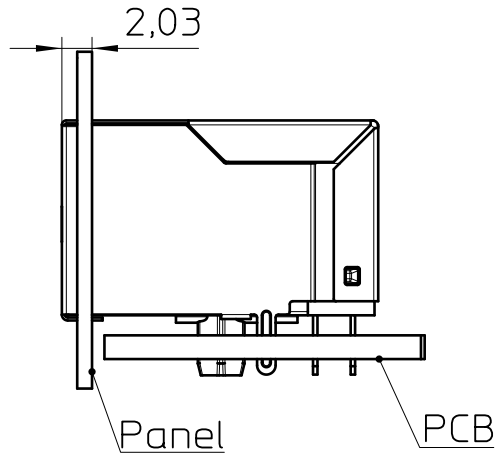
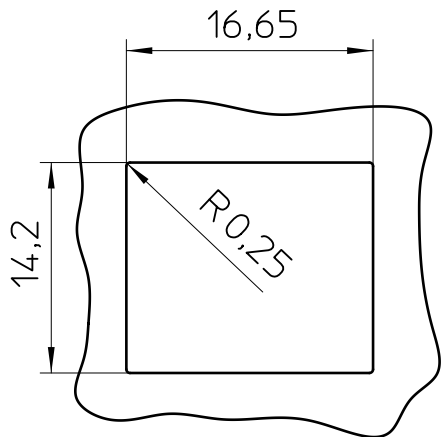


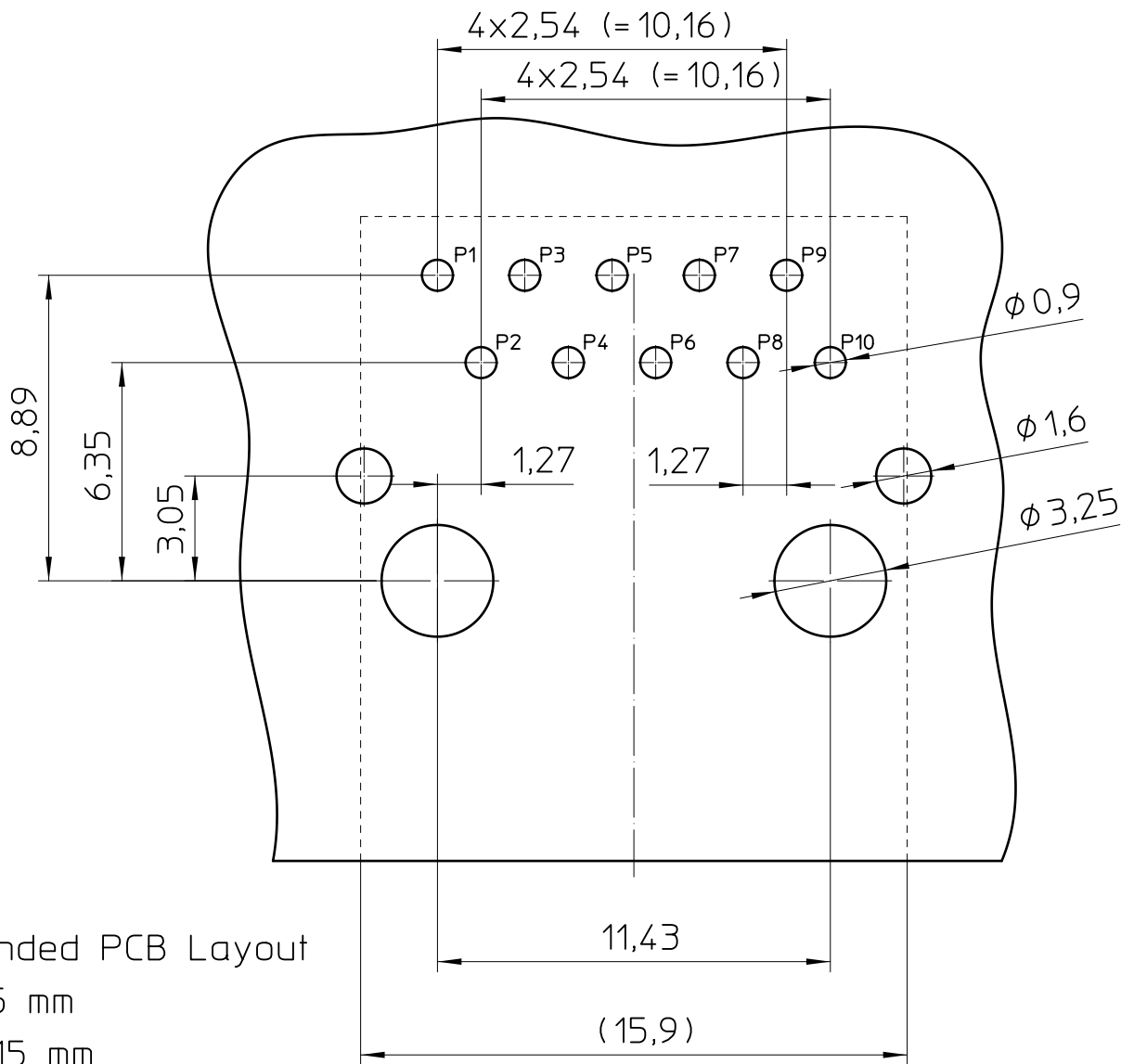
Transfer or duplication of this document as well as the utilisation or communication of its content are not permitted unless express consent is granted. Violations give rise to claims for damages. All rights reserved in case of patent, utility model or design patent registrations. Tolerance specifications do not include clearances inherent in the design.

Weitergabe sowie Vervielfältigung dieses Dokuments, Verwertung und Mitteilung seines Inhalts sind verboten, soweit nicht ausdrücklich gestattet. Zuwiderhandlungen verpflichten zu Schadensersatz. Alle Rechte für den Fall der Patent-, Gebrauchsmuster- oder Designeintragung vorbehalten. Baugrößungsspiel ist in den Toleranzangaben nicht berücksichtigt.

Recommended panel cutout



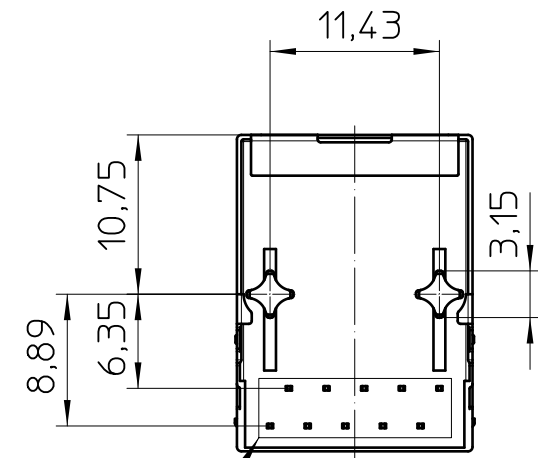
PCB drill hole dimensions (see from component side)



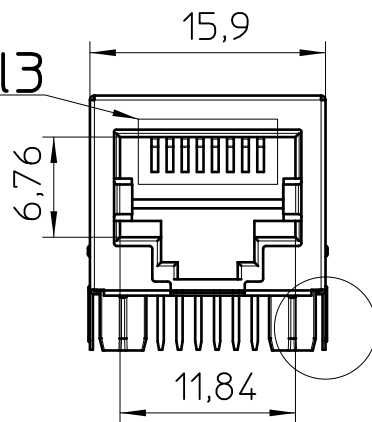
Recommended PCB Layout

Tol: $\pm 0,05$ mm
T=1,60 $\pm 0,15$ mm

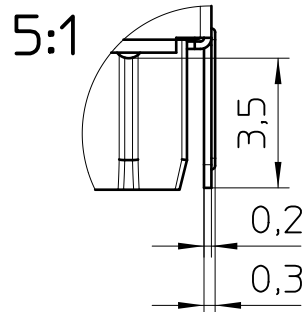
Detail1



Detail3

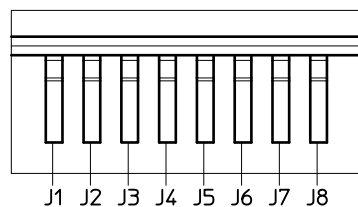


Detail2



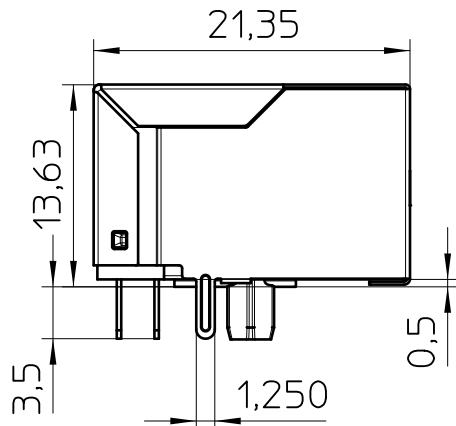
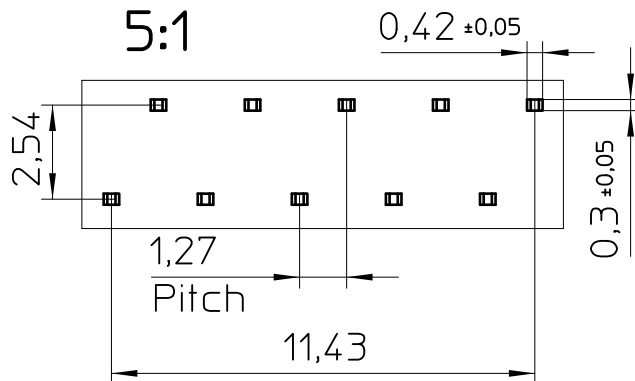
Detail3

5:1



Detail1

5:1



General Tolerances

1 Decimal Place	$\pm 0,25$
2 Decimal Places	$\pm 0,20$
3 Decimal Places	$\pm 0,15$



DIN A3



page 1 of 2

document-no. / ri
01740190 / 00 1664103

date
04.11.2024

document-type
TECDOC 2D_Productfamily

description
CUC-IA1G-J1ST-AB/R4T

scale
2:1

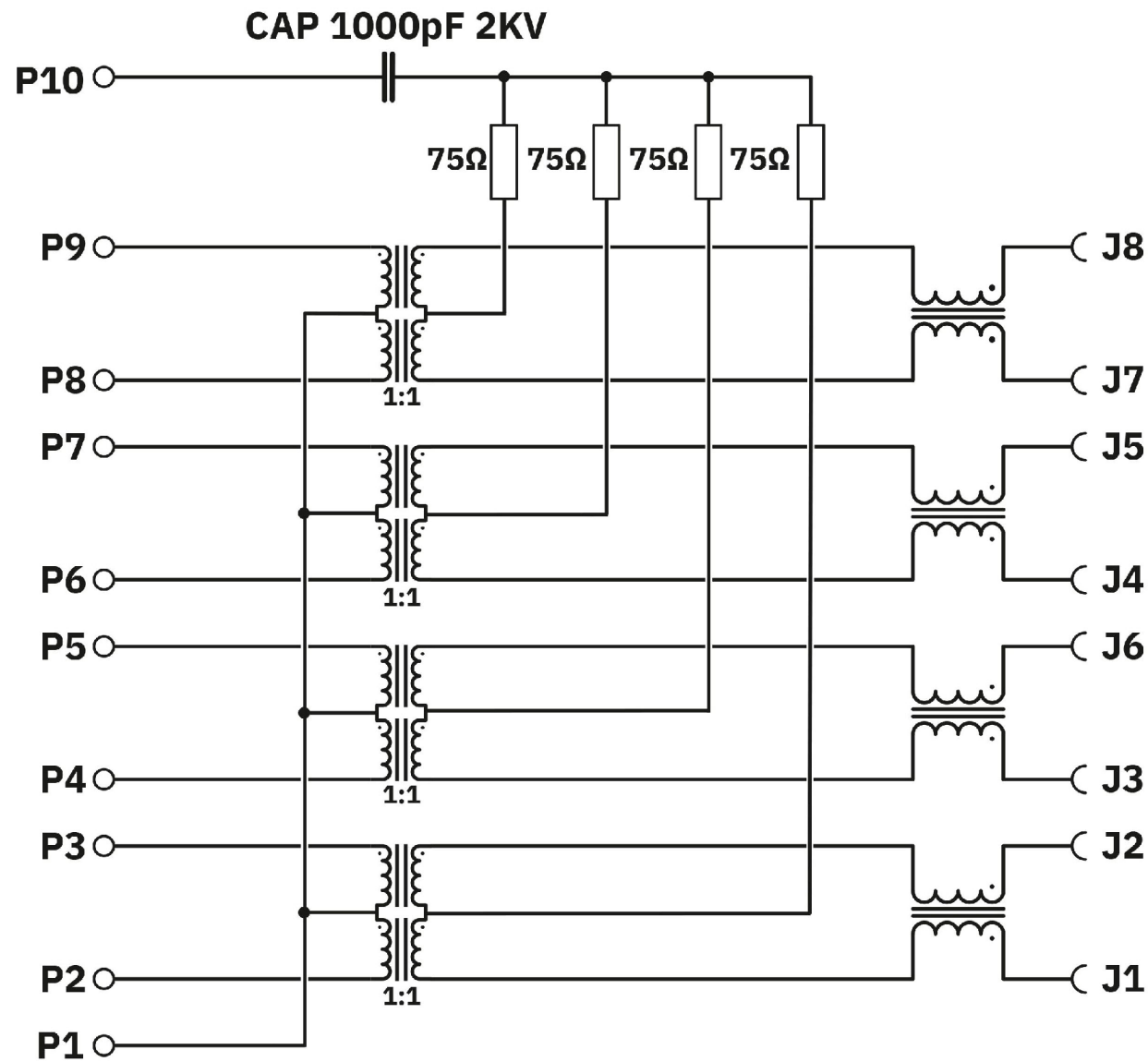
- Simplified representation
- Document excluded
from change process
- Linear dimensions [mm]

Transfer or duplication of this document as well as the utilisation or communication of its content are not permitted unless express consent is granted. Violations give rise to claims for damages. All rights reserved in case of patent, utility model or design patent registrations. Tolerance specifications do not include clearances inherent in the design.

Weitergabe sowie Vervielfältigung dieses Dokuments, Verwertung und Mitteilung seines Inhalts sind verboten, soweit nicht ausdrücklich gestattet. Zuwiderhandlungen verpflichten zu Schadenersatz. Alle Rechte für den Fall der Patent-, Gebrauchsmuster- oder Designeintragung vorbehalten. Bauartbedingtes Spiel ist in den Toleranzangaben nicht berücksichtigt.

PCB SIDE

JACK SIDE



ELECTRONICAL SPECIFICATIONS

1. ACCORDING TO IEEE 802.3

2. TURN RATIO @100KHz: (P2~P3):(J1~J2) = 1:1±5%
(P4~P5):(J3~J6) = 1:1±5%
(P6~P7):(J4~J5) = 1:1±5%
(P8~P9):(J7~J8) = 1:1±5%

3. PRIMARY INDUCTANCE: 350μH MIN @100KHz
0,1V 8mA DC BIAS

4. DC RESISTANCE: 1,2 OHMS MAX

5. INSERTION LOSS: 1-100MHz -1,0dB TYP

6. RETURN LOSS: 1-40MHz -16dB MIN
40-60MHz -12dB MIN
60-80MHz -10dB MIN
80-100MHz -8dB MIN

7. CROSS TALK: 1-100MHz -30dB MIN

8. COMMON TO COMMON
MODE ATTENUATION: 1-100MHz -30dB MIN

9. ISOLATION: PHY SIDE TO LINE SIDE: 2250VDC

- EN ISO 291 23/50

 DIN A3		document-no. / ri 01740190 / 00		article-no. 1664103		scale 2:1		- Simplified representation - Document excluded from change process - Linear dimensions [mm]
		date 04.11.2024		document-type TECDOC 2D_Productfamily				
page 2		of 2		description CUC-IA1G-J1ST-AB/R4T				